REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-12 are pending in this application. Claims 1-12 are amended by the present amendment.

Amendments to the claims find support in the specification as originally filed, at least at page 14, lines 7-25, page 32, lines 6-21, page 45, line 3, to page 46, line 1, and Figure 4. Thus, no new matter is added.

In the Office Action, Claims 1-12 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent 6,336,177 to Stevens. Applicants respectfully traverse that rejection with respect to the amended independent claims.

Claim 1 is directed to an information processing system that includes, in part, means for mapping one of the second and third local memories in part of an effective address space of a first thread executed by a first processor, and means for mapping the other of the second and third local memories in the part of the effective address space of the first thread instead of the one of the second and third local memories, when a processor that executes the second thread is changed from one of the second and third processors to the other of the second and third processors. Further, the first thread accesses the other of the second and third local memories via the part of the effective address space of the first thread to interact with the second thread.

When the processor which executes the second thread is changed from the second processor to the third processor, the contents of the second local memory is not the thread context of the second thread any more. However, the means of the independent claims enables interaction between the first thread and the second thread via the same address region. In other words, the first thread may advantageously interact with the second thread

by merely accessing the same address region, and a first thread may see the local memory of a second thread via the same address at any time. Applicants respectfully submit that Stevens is silent regarding the above described means of the independent claims.

Applicants respectfully submit that Stevens fails to teach or suggest each feature of the independent claims. The Office Action asserts that Stevens, at column 14, lines 36 and 37, column 18, lines 55-63, column 20, lines 52 and 53, and the Abstract, discloses "threads and memory resources can migrate without code modification and/or recompiling, i.e., virtual address relationships among threads are preserved."[1] However, Applicants respectfully submit that Stevens does not teach or suggest a first thread that can see the local memory of a second thread via the same address, and therefore, Stevens does not disclose or otherwise suggest a first thread accessing a memory of another thread via a part of the effective address space of the first thread, as required by the independent claims.

Further, the Office Action asserts that the portions of main memory 114a, 114b of Stevens correspond to the local memories of the present application. However, the information processing system of amended Claim 1 includes not only the local memories but also a shared memory. The local memories of the claimed inventions do not constitute the shared memory, but are a physical memory different from the shared memory. For example, each of the local memories and the shared memory may be mapped in a physical memory space, as shown in Applicants' non-limiting example of FIG. 4. In that example, each processor executes a thread by accessing its own local memory. In other words, the thread context of each thread includes the contents of the local memory of the processor that executes the thread, and each thread can occupy the local memory of the processor that executes the thread. One thread accesses the local memory of the processor that executes the other thread to interact with the other thread. Accordingly, the portions of main memories

[1] Office Action at page 3, lines 3-9.

114a, 114b described by Stevens, may correspond to the claimed shared memory, however, the main memories of Stevens do not correspond to the claimed local memories.

Further, Applicants note that the local memory of Stevens and the claimed local memory of the present invention play different roles. Stevens relates to a multiprocessor of the NUMA type. In the system of Stevens, the "main memory" is divided and located in a plurality of nodes, as indicated by Stevens FIG. 1A, which shows PORTION OF MAIN MEMORY 114A, and which the Office Action appears to assert as being similar to the claimed local memory. Since memory 114A is a main memory, data in the memory can be written or read not only by processors (processes or threads on processors) in the same node but also by all processors. A portion of the memory can be dedicated to a certain process, and another portion can be shared by and accessed from a plurality of processes.

In the present invention, the "main memory" (i.e., shared memory) can be accessed from all processors via a bus. Thus, the main memory described in the specification plays a role similar to the role of Stevens' memory, and a portion of the main memory is dedicated to a certain thread, and another portion is controlled to be shared by a plurality of threads. However, unlike the main memory of Stevens or the main memory described in the specification, the claimed local memory may be dedicated to a thread executed by the processor having the local memory. In particular, the contents (i.e., data) of the local memory belong to the thread. When the execution of a thread on a processor is suspended, the contents of the local memory of the processor are saved, and when the execution of the thread is resumed on another processor, the saved contents are rewritten in the local memory of said another processor. When the execution of the thread on said another processor is started, the rewriting of the contents of the local memory is started, and when the execution of the thread is finished, the contents are saved.

The above-mentioned difference causes a difference in migration.

Stevens describes two migrations: a migration of a memory and a migration of a process. The migration of a memory is to migrate a page from a memory in a node to a memory in another node. Since the page is migrated to a different physical memory, the physical address of the page is actually changed. In other words, according to Stevens, it is necessary to change page tables of all the processes referring to the page so that the entry indicating the physical address of the page before migration indicates the physical address of the page after migration.

The migration of a process is to migrate a process executed by a processor in a node to a different processor in any node (note however, that if there are a plurality of processors in a node, the different processor can be in the same node). Even when the process is migrated from a processor to another processor, data of the memory is not migrated. Since the memory page accessed by the process before migration is the same as the memory page accessed by the process after migration, it is not necessary to change page tables.

In the claimed inventions, the migration of the main memory (i.e., shared memory) is to migrate the contents from a page in the main memory (i.e., shared memory) to a page having a different physical address. Like the migration of the memory of Stevens, page tables of all the threads referring to the page are changed.

However, when a thread migrates according to the claimed inventions, namely, a thread executed by a processor is migrated to a different processor, it is necessary to perform a different processing from that of Stevens. As noted above, the contents of a local memory belong to a thread. Thus, when the thread is migrated to the different processor, the contents of the local memory are also migrated to the local memory of the processor to which the thread is migrated. In this way, the thread and the contents of the local memory the thread uses are migrated at the same time. Therefore, it is necessary to change the page tables of the other threads referring to the local memory of the thread so that the other threads refer to the

local memory of a processor different from the processor before the local memory is migrated. The claimed inventions therefore advantageously map the local memories before and after migration in the same address.

Accordingly, Applicants respectfully submit that Stevens fails to teach or suggest each feature of the claimed invention. For example, Stevens fails to teach or suggest the "means for mapping the other of the second local memory and the third local memory in said part of the effective address space of the first thread . . . the first thread accessing the other of the second local memory and the third local memory via said part of the effective address space of the first thread to interact with the second thread," as recited in independent Claim 1, and as similarly recited in independent Claims 5 and 9.

Therefore, Applicants respectfully submit that independent Claims 1, 5, and 9, and claims depending therefrom, are allowable.

Consequently, in light of the above discussion and in view of the present amendment, this application is believed to be in condition for allowance and an early and favorable action to the effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)

Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Zachary S. Stern
Registration No. 54,719

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